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Revamped Cooling of a Rectangular Shaped Chip Inserting a Highly Conductive Solid: Coupled vs. Uncoupled Conceptions

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Abstract

The performance of highly conductive inserts embedded into a heated chip has been investigated in recent years. The role of the insert was to gather the heat current within the chip and remove it to a low temperature heat sink. The central goal of this study is to invoke several reconsiderations, which results in the plausible reduction of the peak temperature in a heated rectangular chip in comparison with the lowest peak temperature achieved in previous works. It is proved that for the configuration under study with its bottom surface receiving a constant uniform heat flux, the branching patterns of the insert must be avoided, instead the appropriate revisions in the architecture (width, location and cross section area) of the insert are accounted for the simple patterns. An uncoupled analytical solution for predicting the peak temperatures in the rectangular chip containing the cooling insert is also addressed. It is also proved that under the same volume fraction and thermal conductivity of the insert, the peak temperature can be reduced to 2.9 °C, which is 94% below the lowest temperature reported in the archival literature, which was around 50.5 °C.

Keywords: *electronics cooling, rectangular chip, highly conductive insert, minimized peak temperature*

1. Introduction

Heat sinks are usually attached to the surface of electronic packages to create additional surface area for heat removal by conduction, forced convection, natural convection and thermal radiation (Steinberg [1]).

The architecture, namely the collection of configuration, geometry, and geography of flow systems is the persistent movement, struggle, contortion, and mechanism by which the flow structures use the available space for maximum global benefit (Bejan [2]). Searching for a favorable spectrum of optimal architectures for cooling routes embedded in electronic packages is of paramount interest nowadays as stated in References [3-8]. The main concerns are associated with the elevation in operating temperature of electronic components where heat is generated within the body or induced into the outer surfaces. Therefore, numerous researchers have focused their attention on generating the best architecture of cooling routes, such as tree-shaped layouts for fluid flow [3-8] or tree-shaped designs of high-conductivity blades and fibers [9-18] embedded into heat-generating packages.

One fascinating feature of tree networks for fluid flow is that they are not only present in engineering, i.e., man-made architectures [3-8]. Besides, the cooling fluid may have adverse impacts upon the performance of electronic devices and as the sizes of electronic devices become smaller, the traditional convective cooling of these devices can lose its performance. The conductive networks of high-conductivity inserts with no excess work and low occupancy have been proposed to overcome the forgoing concerns associated with fluid flow networks. High conductive cooling inserts become a necessity as the cooling and sensing of smart materials marches toward smaller scales and higher densities of functionality. The challenge that comes with designing the high conductivity inserts is to optimize the architecture of the paths for heat removal from a low conductive electronic component as remarked in References [9-18]). For example, Almogbel and Bejan [10] proposed a non-uniformly distribution of high conductive material and achieved a remarkable improvement in the global performance. Optimal configurations of highly conductive materials at micro- and nano-scales were proposed

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by Gosselin and Bejan [13]. Potvin and Gosselin [15] introduced an evolutionary algorithm with an initial random topology, for optimizing the topology of a heat-generating area cooled by a high thermal conductivity material in contact with a heat sink. Discrete variable cross-section conducting paths of inserts were proposed by Wei et al. [16]. It was shown in this work that the thermal current flows into the high conducting path improved by varying the cross section of the inserts.

Unlike in situations where the chips are envisioned as low conductive media with uniform internal heat generation [8-16], Mazloomi et al. [18] have considered a rectangular chip where the heat is induced at the bottom surface of the chip. Throughout the optimization of highly conductive insert architecture for cooling a rectangular chip, the authors have shown that branching pattern of inserts reduces the excess temperature of the chip. Despite their research is a significant reference in design, there are several issues and alternative solutions that are essential for improving the impact of highly conductive inserts on the maximum temperature of the electronic chip under study. For example, it is shown that the branching patterns (tree shaped networks) embedded in the chip are not reasonable for heat removal from an electronic chip where its bottom surface is subjected to uniform heat flux. However, a volume that generates heat at every point within the body can be well cooled by distributing the cooling stream through the volume as a tree-shaped network.

The main objective of the present study is to revisit the work of Mazloomi et al. [18] and 1) change the location of the insert, 2) change the location of the heat sink, 3) design the insert with variable cross section and 4) explore alternative simplified solutions. It will be demonstrated that by implementing the foregoing reconsiderations, the peak temperature of the rectangular chip can be reduced by 100% in comparison with the findings in [28].

2. Physical System

Consider the ensemble of an electronic package illustrated in Figure 1a. One part of the ensemble is a rectangular chip with low thermal conductivity k_l and the other part is a rectangular insert made of a material with high thermal conductivity k_h. The front view of the electronic package ensemble is sketched in Figure 1b. The dimensions of the rectangular chip are h= 4.5 mm, w_1 = 9 mm and l_1=*20* mm, while the dimensions for the insert t, w_2, l_2 are considered as variable. The distance between the insert and the bottom surface of the rectangular chip, e, is taken as a variable also. The heat current within the rectangular chip originates from the bottom surface, which is subjected to a uniform heat flux of magnitude, q_o'' = 20,000 W/m^2. Owing to the mismatch in thermal conductivities, $k_h >> k_l$, the highly conductive insert is responsible for gathering the heat current within the rectangular chip and removing it to a minimum-temperature sink. The sink sketched in Figure 1b with dimensions t, w_2 is attached to the faces of the rectangular chip and maintained at the minimum temperature level, T_{min} = 0 $^\circ C$ caused by either forced or natural convection. The remaining faces of the rectangular chip are thermally insulated. For the sake of simplicity, the thermal properties of the materials are assumed invariant with temperature.

The total volume occupied by the highly conductive insert, V_{k_h}, is fixed giving rise to the constraint (1)

$$V_{k_h} = L_1 W_1 t = Const. \tag{1}$$

and the constraint (2)

$$\phi = \frac{V_{k_h}}{V} = \frac{V_{k_h}}{V_{k_h+k_l}} = Const. \tag{2}$$

where $V = V_{k_h+k_l}$ is the total volume occupied by the ensemble in Figure 1a and ϕ represents the volume fraction occupied by the insert.

Under the stated conditions, the objective of the study is to minimize the peak temperature in the rectangular chip (see Figure 1a) by varying the architecture of the insert under the influence of constraint (2).

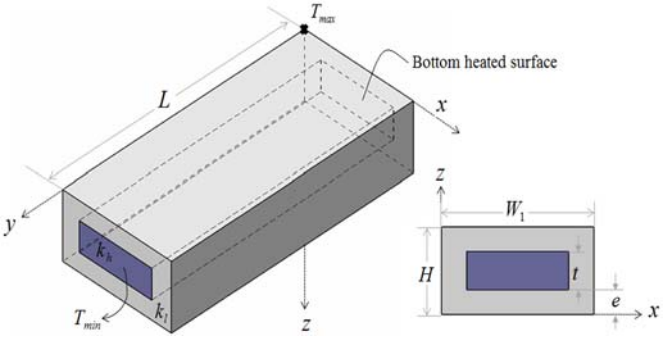

Figure 1. Geometry and coordinate system for an ensemble showing an insert embedded into a rectangular chip

3. Mathematical Model

The coupled, 3-D steady-state heat conduction equations in the rectangular chip identified by the subscript (l) and the insert identified by the subscript (h) are

$$\frac{\partial^2 T_h}{\partial x^2} + \frac{\partial^2 T_h}{\partial y^2} + \frac{\partial^2 T_h}{\partial z^2} = 0 \tag{3a}$$

$$\frac{\partial^2 T_l}{\partial x^2} + \frac{\partial^2 T_l}{\partial y^2} + \frac{\partial^2 T_l}{\partial z^2} = 0 \tag{3b}$$

respectively. The applicable boundary conditions are: 1) prescribed temperature at the sink, T_{min}, 2) constant heat flux, q_o'', at the bottom of the rectangular chip, 3) thermal insulation condition at the remaining faces of the rectangular chip, $\frac{\partial T}{\partial n} = 0$, and 4) coupled temperature and coupled heat flux at the interface between the sub-domain (l) and the sub-domain (h), (implying continuity in temperature and heat flux). That is, $T_h = T_l$ and $\left(k\frac{\partial T}{\partial n}\right)_k = \left(k\frac{\partial T}{\partial n}\right)_l$.

4. Numerical Computation

Using the Finite Element Method (FEM) (Zienkiewicz et al. [19]), the system of two coupled partial differential equations (3a)–(3b) subject to the proper boundary conditions was solved numerically with COMSOL Multiphysics version 3.5 [20],

along with the numerical solver UMFPACK (Davis [21]). COMSOL is a commercial code containing an advanced software package for modeling physical systems describable by a system of partial differential equations.

In the mesh, the layout of finite elements is non-uniform in the x, y and z coordinates, and varied from one geometry to the next. As is customarily done, the appropriate mesh size is determined by means of successive refinements, increasing the number of finite elements between consecutive mesh sizes, until the stringest convergence criterion is satisfied.

When the dimensions of the rectangular chip and the insert are different in height, namely $W_1 = W_2 = W$ and $L_1 = L_2 = L$, the 3-D domain of the ensemble in Figure 1a is reduced to a 2-D domain in y-z plane as depicted in Figure 2. Note that the outer surfaces of the rectangular chip and the insert (excluding the sink) are thermally insulated. Because the thermal conductivity ratio $k_h >> k_l$, it is natural to postulate the following assumptions:

1- The heat current is in the z-direction of the rectangular chip while the heat current in the insert is in the x-direction.

2- The heat current at the lower region of the rectangular chip (below the insert) which is originated from the bottom surface of the chip is extracted via the highly conductive insert such that the heat current in the upper chip region (above the insert) vanishes.

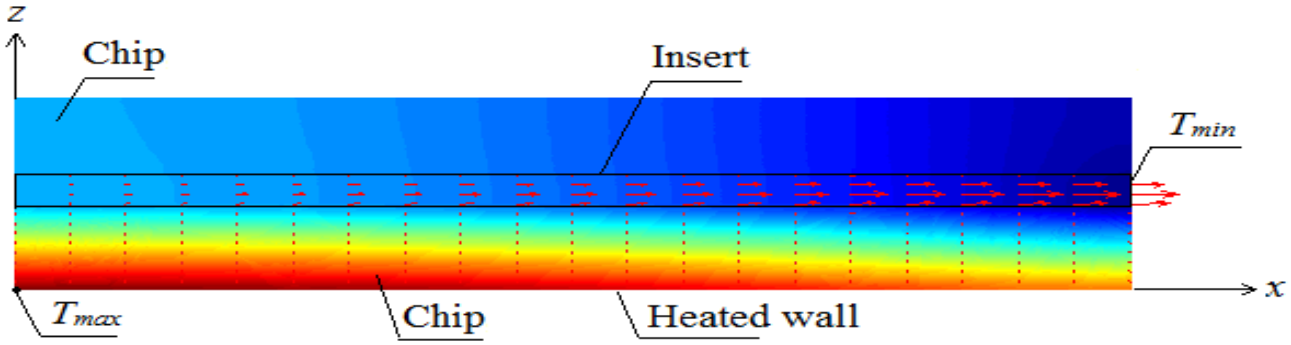

Figure 2. Heat flux vectors for the ensemble when $W_2 = W_1$ and $L_2 = L_1$

In view of these simplifications, the uncoupled, 1-D heat conduction equation in the (h) sub-domain is

$$k_h A_h \frac{d^2 T_h}{dy^2} + q_o'' W = 0; \tag{4}$$

subject the boundary conditions

$$\frac{dT_h}{dy} = 0 \ at \ y = 0; \quad T_h = 0 \ at \ y = L \tag{4a}$$

Also, the uncoupled, 1-D heat conduction equation in the (l) sub- domain is

$$\frac{d^2 T_l}{dz^2} = 0; \tag{5}$$

along with the boundary conditions

$$-k_l \frac{dT_l}{dz} = q_o'' \ at \ z = 0; \quad T_h = T_l \ at \ z = e \tag{5a}$$

where $A_h = W_2 t$ is the cross section area of the insert.

Solving the two ordinary differential equations (4) and (5), the temperature distributions in the (h) and (l) sub-domains are written as

$$T_h(y) = \frac{1}{2k_h t} q_o'' \left(L^2 - y^2\right) \tag{6}$$

$$T_l(z) = \frac{1}{k_l} q_o'' \left(e - z\right) + T_h \tag{7}$$

Knowing that the peak temperature, T_{max}, occurs at the origin (see Figure 2), then substituting $y = z = 0$ in eq. (7) provides

$$T_{\max} = \left(R_h + R_l\right) q_o'' LW \tag{8}$$

where $R_h = \frac{L^2}{2k_h \phi V_{k_h + k_l}}$ denotes the thermal resistance of the insert and $R_l = \frac{e}{k_l LW}$ stand for the thermal resistance of the rectangular chip.

5. Results and Discussion

In this section, first and foremost, the revamped results addressing the improved architecture of the insert and the corresponding minimum peak temperature, $T_{max,min}$, are presented with reference to the various reconsiderations made in the so-called optimal architecture reported in Ref.-[28]. The one-to-one comparison reveals that by implementing the suggested revisions, the peak temperature in the rectangular chip is significantly reduced.

5.1 Changing the insert width ratio

The effects of the insert width ratio, W_2/W_1, on the peak temperature T_{max} in the rectangular chip are shown in Figure 3 for two cases characterized by $\phi = 0.11$ and 0.22, when $L_2 = L_1$ and $k_h/k_l = 500$. It is evident that the peak temperature T_{max} is reduced when W_2 approaches W_1, such that the minimum peak temperature $T_{max,min}$ is obtained under the conditions $W_2 = W_1$ for both cases associated with $\phi = 0.11$ and 0.22, which have been both considered in Ref [28]. However, the above-mentioned favorable fact is somehow hidden in the results reported in Ref. [28], because the two simple patterns (without any branches) dealing with different width ratio, $W_2/W_1 = 0.5$ and $W_2/W_1 = 1$ in Ref. [28] are with unequal values of volume fraction, $\phi = 0.11$ and 0.22, respectively. Therefore, no comparison could be made among the two cases involving $W_2/W_1 = 1$ and $W_2/W_1 < 1$ for the same ϕ, so as to reveal the advantage for increasing W_2/W_1. The temperature distribution for the ensemble is depicted in Figure 4 for the cases of $W_2/W_1 = 0.5$ and $W_2/W_1 = 1$ when $\phi = 0.11$ and $k_h/k_l = 500$. It is observed

that the peak temperature $T_{max} = 55.4\,^{\circ}C$ in the case of $W_2/W_1 = 1$ is lower than $T_{max} = 67.71\,^{\circ}C$ in the case of $W_2/W_1 = 0.5$, which has been considered in Ref. [28]. The second consequence for disregarding the favorable effect of increasing W_2/W_1 on the peak temperature T_{max} in the rectangular chip addressed in Ref. [28] is discussed in the next sub-section.

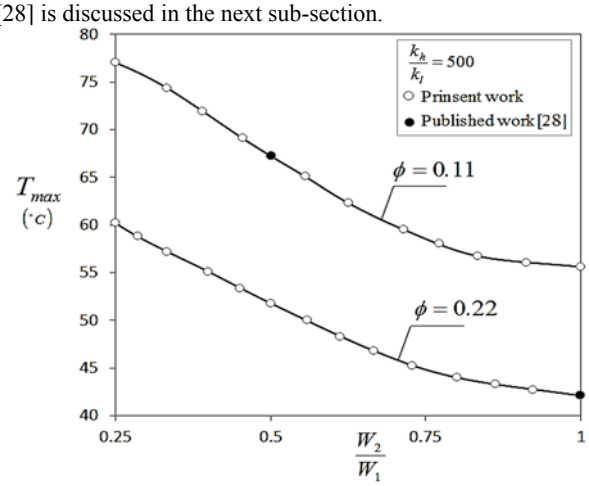

Figure 3. Effect of the insert width ratio, W_2/W_1 , on the peak temperature of the rectangular chip

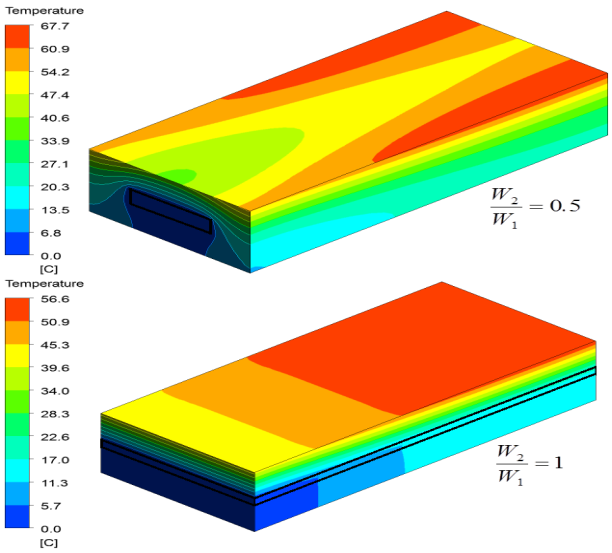

Figure 4. Temperature distribution in the ensemble for two cases having W_2/W_1= 0.5 and W_2/W_1= 1, along with ϕ = 0.11 and k_h/k_l = 500

5.2 Simple pattern or branching pattern?

The underlying idea in Ref. [28] is to propose several branching patterns of the insert and recommending that the branching patterns can result in superior results than the simple pattern of the insert assigning any branches. This conclusion is an alternative consequence of disregarding the favorable effect of increasing W_2/W_1 on the peak temperature T_{max} in the rectangular chip examined in Ref. [28] and considering the two cases of $W_2/W_1 = 0.5$ and $W_2/W_1 = 1$ at unequal values of $\phi = 0.11$ and 0.22, respectively. In other words, to prove the superiority of the branching pattern over the simple branching in Ref. [28], the peak temperatures T_{max} of the present branching in the case of $\phi = 0.11$ have been compared against those associated with two branching patterns when W_2/W_1= 0.5 and ϕ = 0.11 and when W_2/W_1= 1 and ϕ = 0.22. If the peak temperatures T_{max} of the branching had been compared with those of the simple branching pattern in the cases of W_2/W_1= 1 and the same ϕ = 0.11, the advantage of the branching over the simple pattern would not have been achieved. This statement is evident by inspecting Table 1, where the efficiency of the branching pattern studied in Ref. [28] on reducing the peak temperature T_{max} is evaluated in comparison with the simple case for W_2/W_1= 1 and the same ϕ = 0.11 (T_{max} = 55.4 $^{\circ}C$). As it is observed, the branching patterns with $n < 10$ (n is the number of branches) are inefficient in comparison with the simple branching of W_2/W_1= 1 and the same ϕ while the branching with $n > 10$ has an insignificant advantage over the simple branching pattern. In other words, we may be able to conclude that the branching patterns of the insert, aside with complexity and inconvenient applicability does not possess superior thermal performance in the configuration under study where the heat flux is induced at the bottom surface of the rectangular chip.

To end the sub-section, it is worth noting that the branching patterns and the cooling networks are chiefly appropriate or even essential for a gathering the heat current in the media that generates heat at every point within the body (see Refs. [18-27]). In the case of the rectangular chip under study where the heat current in the body is originated from the outer surfaces of the rectangular chip subjected to uniform heat flux, not only the branching patterns are not reasonable, but also the location of the insert platform must be close enough to the subjected surfaces to the heat flux. This issue is discussed more clearly in the next sub-section.

Table 1: Comparison of the peak temperature in the rectangular chip corresponding to different number of branches [28] and the increase (+)/decrease (-) percentage of maximum temperature relative to the simple pattern of the insert when $W_2 = W_1$, $L_2 = L_1$, e = 2 mm, k_h/k_l = 500 and ϕ = 0.11

N (number of branches)	T_{max} in [28] (branching)	$\frac{T_{max}(\text{branching}) - T_{max}(\text{simple})^*}{T_{max}(\text{branching})}$ (%)
2	68.589 $^{\circ}C$	+18.9
5	58.943$^{\circ}C$	+5.7
10	55.813$^{\circ}C$	+0.38
15	55.321$^{\circ}C$	--0.5
20	54.951$^{\circ}C$	--1.18

*: $W_2/W_1 = L_2/L_1$= 1, e = 2 mm, T_{max} = 56.6 $^{\circ}C$

4.3 Changing the insert placement

According to Eq. (8), there is an excessive thermal resistance associated with the bottom part of the rectangular chip located between the insert and the heated surface. This means that the assumption made in Ref. [28] in reference that the insert platform is mounted at the middle of the rectangular chip is not reasonable. Since the thermal conductivity of the rectangular chip is negligible, the related thermal resistance has a detrimental effect on increasing the peak temperature T_{max} and must be essentially avoided. This resistance can be simply removed by approaching the insert platform into the bottom surface of the chip where it is exposed to heat flux. To clarify the foregoing comment, the role played by the distance between the insert and the bottom surface of the chip, e, on the magnitude of the peak temperature T_{max} is displayed in Figure 5, when k_h/k_l = 500, $W_2 = W_1$, $L_2 = L_1$, for two distinct cases of ϕ = 0.11 and 0.22. The influence of k_h/k_l on reducing the peak temperature T_{max} which is not documented in Ref. [28], is also depicted in Figure 6, when e = 0. As witnessed in the tandem of Figures 5 and 6, there is an excellent agreement between the analytical and numerical results.

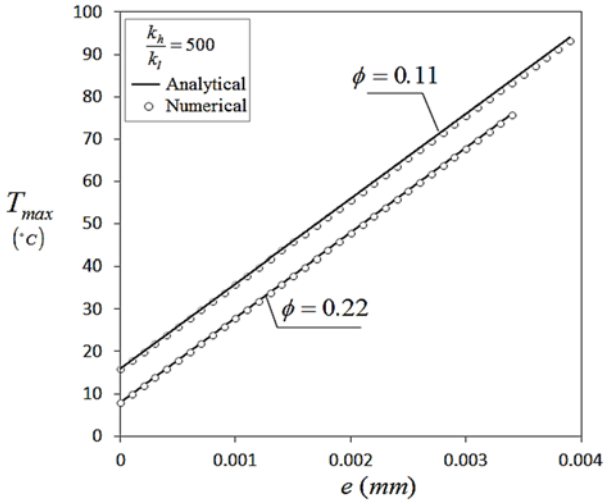

Figure 5. Effect of the distance "*e*" between the insert and the bottom surface of the rectangular chip on the peak temperature when W_2/W_1 = 1 and L_2/L_1= 1

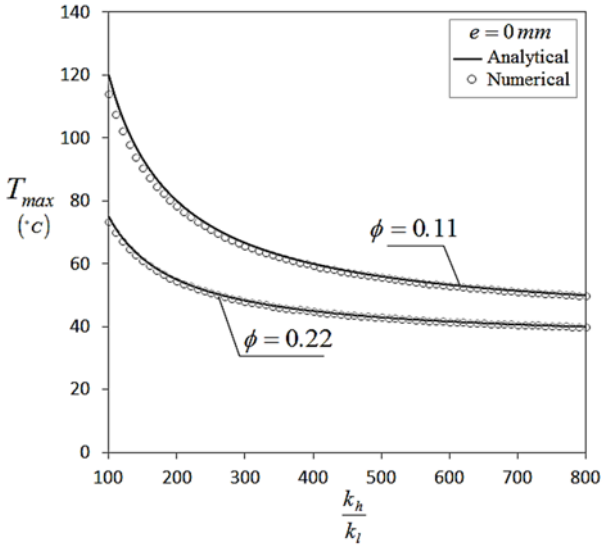

Figure 6: Influence of k_h/k_l on reducing the peak temperature given W_2/W_1= 1, L_2/L_1= 1 and e = 0.

To further appreciate the reconsideration made in the present sub-section, the 2-D temperature distributions in the rectangular chip (in z-y plane) are presented in Figure 7 when $W_2 = W_1$, $L_2 = L_1$, ϕ = 0.11and k_h/k_l = 500. The comparison made in this figure revolves around two cases: (a), the insert is amounted above the heated surface of the rectangular chip (e = 0) and (b), the insert is mounted at the middle of the rectangular chip (e = 2mm). Compared with the case (b), it is evident that the peak temperature in the case (a), with T_{max} = 55.6 °C, is 71.6 % lower than the one in case (b), where T_{max} = 15.8 °C. Besides, other insert architectures, where the cooling channel (insert) is partially mounted on the bottom surface may nearly provide the same peak temperature T_{max}, when $L_2 = L_1$, ϕ = 0.11and k_h/k_l = 500. The foregoing insert architectures are depicted in Figure 7 on the z-x plane where the sink is located. For purposes of design and manufacturing of electronic packages, the insert can be mounted close to the heated surface, instead of being mounted above the bottom surface.

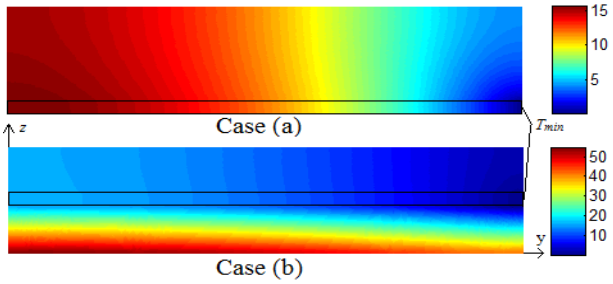

Figure 7: Comparison between the 2-D temperature distribution in the rectangular chip (in the *z*-*y* plane) for two cases: case (a), the insert is mounted above the heated surface of the chip (e = 0) and case (b), the insert is mounted at the middle of the rectangular chip (e = 2mm).

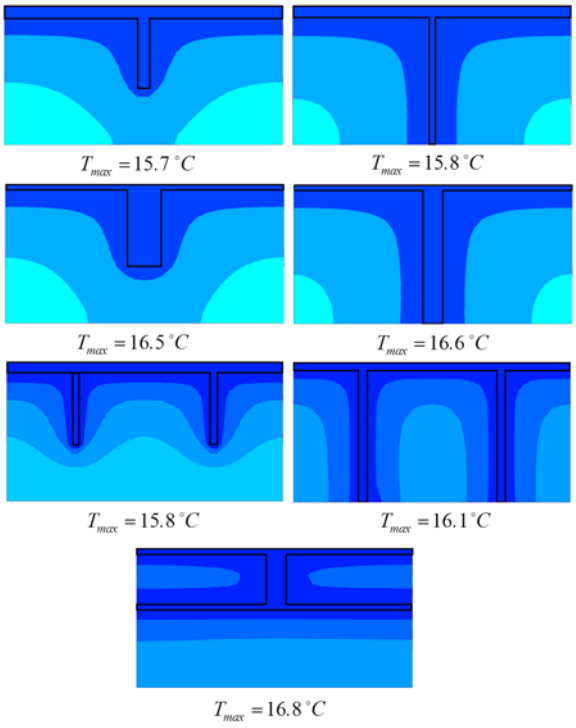

Figure 8: Several architectures with different shapes of insert cross section and almost the same peak temperature relative to the simple pattern having rectangular cross section, keeping $L_2 = L_1$, ϕ = 0.11and k_h/k_l = 500

5.4 Changing the location of the heat sink

So far we have managed to remove the thermal resistance associated with the chip materials by equalizing the insert width to the width of the rectangular chip and eliminating the separation between the heated surface of the rectangular chip and the insert platform. Therefore, the only thermal resistance that the heat current encounters is the one associated with the insert. However the thermal conductivity of the insert, k_h, is considerably higher in comparison with that of the rectangular chip, k_l . Further, it is worthy to focus on reducing the above-mentioned resistance in order to cut down the peak temperature T_{max} significantly. The present and the next sub-sections deal with the foregoing dilemma.

According to Eq. (8), it is observable that the thermal resistance of the insert, $R_h = \dfrac{L^2}{2k_h\,\phi V_{k_h+k_l}}$ is proportional to L^2. Recognizing that in the present study, as well as in Ref. [28], $L > W$, it is natural to reduce the mentioned resistance to $R_h = \dfrac{W^2}{2k_h\,\phi V_{k_h+k_l}}$ by mounting the heat sink on the face of the rectangular chip normal to the x axis unlike the previous architectures where the heat sink was mounted on the face of the rectangular chip normal to the y axis. Applying the preceding reconsideration in the location of the heat sink, the peak temperature $\widetilde{T}_{\max}$ is diminished from 15.8 $^\circ C$ to a surprising 3.2 $^\circ C$, This means a 79.8% reduction in the peak temperature T_{max}, when $W_2 = W_1$, $L_2 = L_1$, $e = 0$, $\phi = 0.11$, $k_h/k_l = 500$ are specified.

5.5. Varying the cross-section area of the insert

Another avenue for reducing the insert thermal resistance is varying the cross section of the insert in the heat current direction at the insert. Let us suppose that $W_2 = W_1 = W$, $L_2 = L_1 = L$, $e = 0$ and the heat sink is located on the face of the rectangular chip normal to the x axis. The cross section area of the insert is $A_x(y) = t(x)\,L$. Further, suppose that the thickness profile of the insert, is described by the power equation $t(x) = a\,x^n$. When $n < 1$, the solution of Eq. (4) in terms of the x coordinate with $A_h(x) = c\,x^n\,L$ is

$$T(x) = \frac{q_o''}{(2-n)\,k_h c}\left(W^{2-n} - x^{2-n}\right) \qquad (9)$$

Considering the constraint (4) gives $a = \dfrac{\phi H(n+1)}{W^n}$ and substituting "a" in Eq. (9), the peak temperature results in

$$T_{max} = \frac{1}{(2-n)(1+n)}\frac{W^2\left(q_o'' LW\right)}{\phi k_h V_{k_h+k_l}} \qquad (10)$$

Next, calculating $\dfrac{\partial \widetilde{T}_{\max}}{\partial n} = 0$ supplies the best temperature profile that minimizes the peak temperature $T_{max,min}$. Correspondingly, this gives n_{opt} = ½ and $T_{max,min} = \dfrac{(4/9)W^2\left(q_o'' LW\right)}{\phi k_h V_{k_h+k_l}}$. Comparing this expression with the minimized peak temperature obtained by the previous sub-section, $T_{max,min} = \dfrac{2W^2\left(q_o'' LW\right)}{\phi k_h V_{k_h+k_l}}$, the reconsideration made in the present sub-section produces a 11% reduction in the peak temperature T_{max}. The 2-D temperature distributions for the ensemble having an insert of variable cross section areas $A_h(y) = (3/2)\,\phi\,H\,WL\left(\dfrac{y}{L}\right)^{1/2}$ and $A_h(x) = c\,L\,y^{1/2}$, for the two layouts are depicted in the pair of Figures 9a and 9b, respectively. Here, the heat sink is located in z-x and z-y plane.

It is observed that by implementing the stated reconsiderations along with the alternative solutions, the peak temperature is reduced to $\widetilde{T}_{\max,\,\min}$ = 2.9 $^\circ C$, which is 94% below the lowest peak temperature reported in Ref. [28]. In addition, $\widetilde{T}_{\max,\,\min}$ = 50.5 $^\circ C$, with the same values for ϕ and k_h/k_l are assigned.

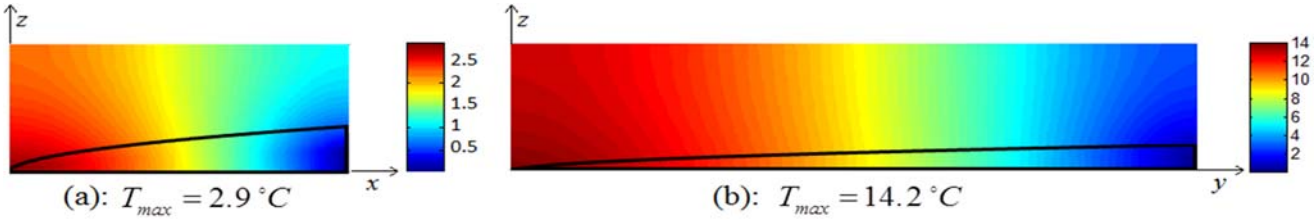

Figure 9: 2-D temperature distributions for the ensemble with an insert of variable cross section area for two layouts: (a) $A_h(y) = (3/2)\,\phi\,H\,WL\left(y/L\right)^{1/2}$ and (b) $A_h(x) = c\,L\,y^{1/2}$, where the heat sink is located in (a): the z-x and (b): the z-y plane

6. Conclusions

We conducted a study related to the best placement of a highly conductive insert into a rectangular chip where its bottom surface has a prescribed uniform heat flux. The role of the insert was to gather the heat current within the chip and remove it to a minimum temperature heat sink. Several reconsiderations were directed at the minimization of the peak temperature in the chip by way of determination of the most efficient architecture of the insert. Throughout the first reconsideration, we proved that, when the widths of the insert and chip are equal, the peak temperature of the chip is lower in comparison with the case that the width of the insert is half of the width of the chip under the same volume fraction of the insert. It was also discovered in the second reconsideration that under the same volume fraction of the insert, the branching pattern is not superior to the simple pattern for the configuration under study. During the third reconsideration, we proved that the assumption that the insert platform is mounted at the middle of the chip must be strongly reconsidered and we recommended that the insert platform must be mounted close enough to the heated bottom surface of the chip. Implicit to the final reconsideration, we demonstrated that the location of the heat sink must be changed.

Proposing an analytical solution to predict the peak temperature in the rectangular chip for the simple patterns was an important aspect addressed in the present work.

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